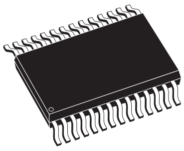
TDA7719

3 band car audio processor

Features

- Input multiplexer
  – Multiple input configuration for different application
- Loudness
  – 2nd order frequency response
  – Programmable center frequency
  – 15 dB with 1 dB steps
  – Selectable high frequency boost
  – Selectable flat-mode
- Volume
  – +15 dB to -15 dB with 1 dB step resolution
  – Soft-step control with programmable blend times
- Bass
  – 2nd order frequency response
  – Center frequency programmable in 4 steps
  – Q programmable 1.0/1.25/1.5/2.0
  – DC gain programmable
  – -15 to 15 dB range with 1 dB resolution
- Middle
  – 2nd order frequency response
  – Center frequency programmable in 4 steps
  – Q programmable 0.5/0.75/1.0/1.25
  – -15 to 15dB range with 1dB resolution
- Treble
  – 2nd order frequency response
  – Center frequency programmable in 4 steps
  – -15 to 15dB range with 1dB resolution
- Speaker
  – 4 independent soft step speaker controls
  – 0dB to -79dB with 1dB steps
  – Direct mute
- Subwoofer
  – 2nd order low pass filter with programmable cut off frequency
  – 2 independent soft step level control,
- Mute functions



TSSOP28

  – Direct mute
  – Digitally controlled SoftMute with 4 programmable mute-times
- Offset detection
  – Offset voltage detection circuit for on-board power amplifier failure diagnosis
- Level meter
  – Provide rectified level voltage of main source signal (before loudness)
- Rear seat selector
  – Full source selector for rear seat output
- Mixing selector

Description

The TDA7719 is a high performance signal processor specifically designed for car radio applications. The device includes a high performance audioprocessor with fully integrated audio filters and new Soft Step architecture. The digital control allows programming in a wide range of filter characteristics. By the use of BCMOS-process and liner signal processing low distortion and low noise are obtained.

Table 1. Device summary

Order code	Package	Packing
TDA7719	TSSOP28	Tube
TDA7719TR	TSSOP28	Tape and reel

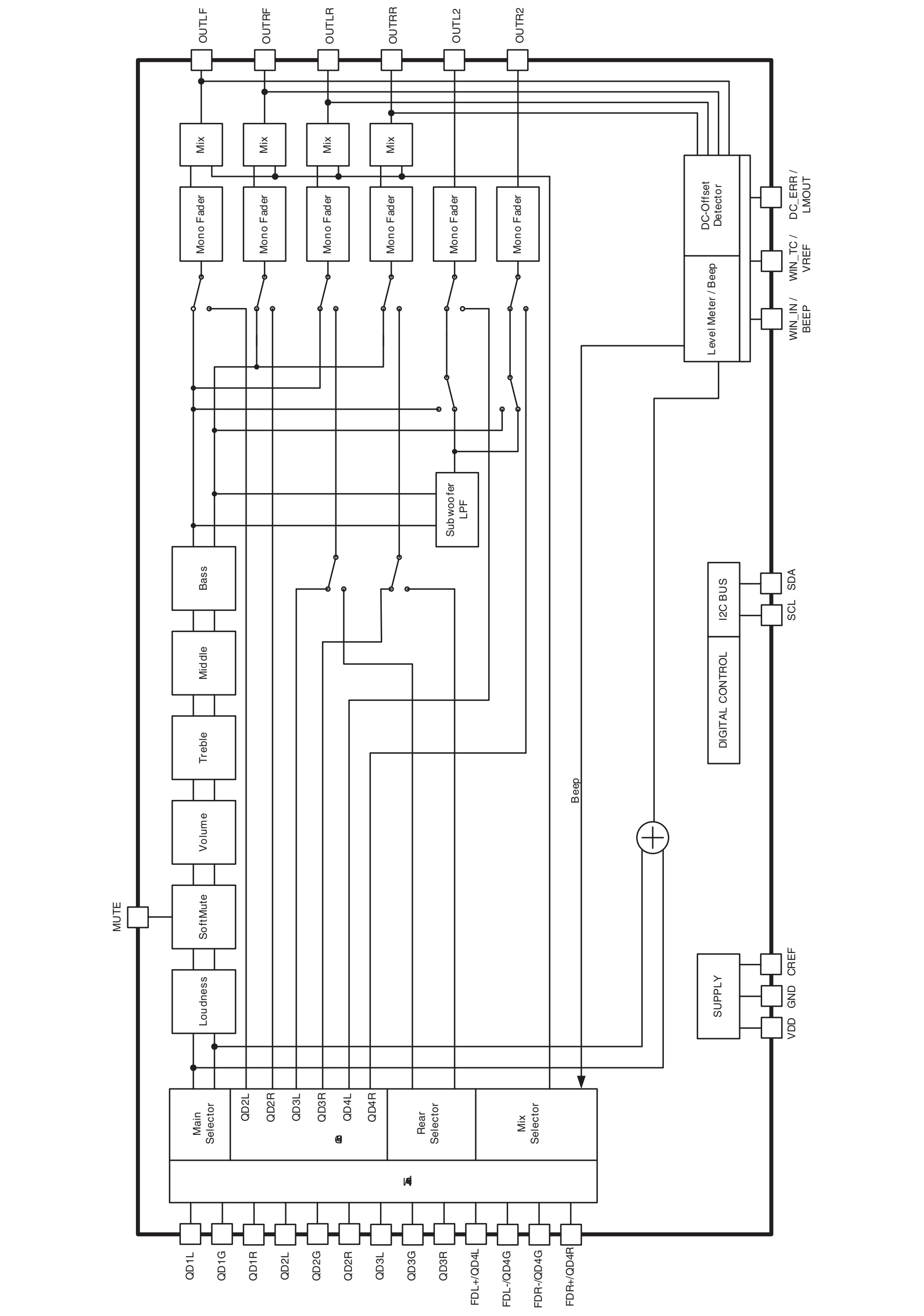
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1 Block circuit diagram

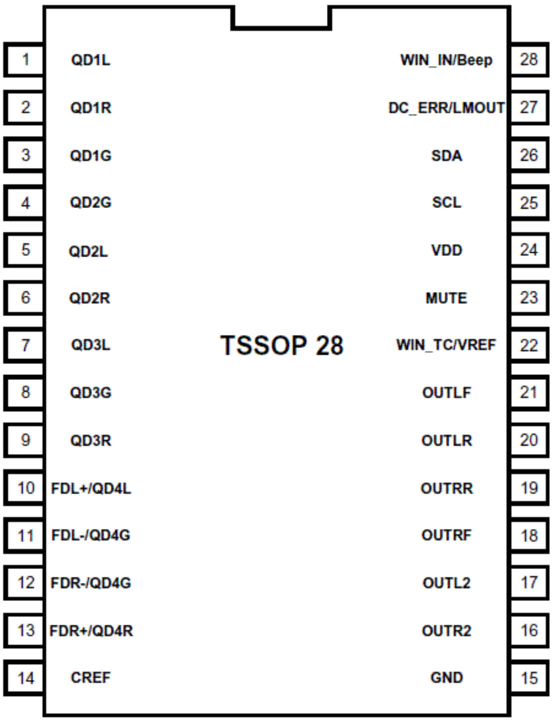
Figure 1. Block circuit diagram



2 Pin description

2.1 Pin connection

Figure 2. Pin connection (top view)



2.2 Pin description

Table 2. Pin description

No.	Pin name	Description	I/O
1	QD1L / SE1L / MD3+	QD1 left input or SE1 left or MD3 positive input	I/O
2	QD1R / SE1R / MD3-	QD1 right input or SE1 right input or MD3 negative input	I/O
3	QD1G / SE2L	QD1 common input or SE2 left input	I/O
4	QD2G / SE2R	QD2 common input or SE2 right input	I/O
5	QD2L / SE3L	QD2 left input or SE3 left input	I/O
6	QD2R / SE3R	QD2 right input or SE3 right input	I/O
7	QD3L	QD3 left input	I/O
8	QD3G	QD3 common input	I/O
9	QD3R	QD3 right input	I/O

Table 2. Pin description (continued)

No.	Pin name	Description	I/O
10	QD4L / FD4L+ / SE4L / MD1+	QD4 left input or FD4L positive input or SE4 left input or MD1 positive input	I/O
11	QD4G / FD4L- / SE4R / MD1-	QD4 common input or FD4L negative input or SE4 right input or MD1 negative input	I/O
12	QD4G / FD4R- / SE5L / MD2-	QD4 common input or FD4R negative input or SE5 left input or MD2 negative input	I/O
13	QD4R / FD4R+ / SE5R / MD2+	QD4 right input or FD4R positive input or SE5 right input or MD2 positive input	I/O
14	CREF	Reference capacitor	O
15	GND	Ground	S
16	OUTR2	Subwoofer output / 2nd right output	O
17	OUTL2	Subwoofer output / 2nd left output	O
18	OUTRF	Front right output	O
19	OUTRR	Rear right output	O
20	OUTLR	Rear left output	O
21	OUTLF	Front left output	O
22	WinTC / VREF	DC offset detector filter or Vref output	O
23	MUTE	I^2C bus data	I/O
24	VDD	Supply	S
25	SCL	I^2C bus clock	I
26	SDA	I^2C bus data	I/O
27	DC_ERR / LMOUT	DC offset detector output or Level meter output	O
28	WIN_IN / Beep	DC offset detector input or Beep input (Mono Single-Ended input)	I

3 Electrical specifications

3.1 Thermal data

Table 3. Thermal data

Symbol	Description	Value	Unit
$R_{th\text{-}j\ amb}$	Thermal resistance junction to ambient	114	°C/W

3.2 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_S	Operating supply voltage	10.5	V
V_{in_max}	Maximum voltage for signal input pins	7	V
T_{amb}	Operating ambient temperature	-40 to 85	°C
T_{stg}	Storage temperature range	-55 to 150	°C

3.3 Electrical characteristics

V_S = 8.5 V; T_{amb}= -40 to 85 °C; R_L= 10 kΩ; all gains = 0 dB; f = 1 kHz; unless otherwise specified

Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Supply						
V_s	Supply voltage		7.5	8.5	10	V
I_s	Supply current			35		mA
Input selector						
R_{in}	Input resistance	All single ended inputs(1)	70	100	130	kΩ
V_{CL}	Clipping level	Input gain = 0 dB		2		V_{RMS}
S_{IN}	Input separation			100		dB
Differential stereo inputs						
R_{in}	Input resistance	Differential	70	100	130	kΩ
CMRR1	Common mode rejection ratio for main source	V_{CM}=1 VRMS@ 1 kHz	46	60		dB
		$V_{CM=}$1 VRMS@ 10 kHz	46	60		dB
CMRR2	Common mode rejection ratio for 2nd source	V_{CM}=1 VRMS@ 1 kHz	46	60		dB
e_{No}	Output noise @ speaker outputs	20 Hz-20 kHz, A-weighted; all stages 0dB		12		µV

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Loudness control						
A_{MAX}	Max attenuation			15		dB
A_{STEP}	Step resolution			1		dB
f_{Peak}	Peak frequency	f_{P1}		400		Hz
		f_{P2}		800		Hz
		f_{P3}		2400		Hz
Volume control						
G_{MAX}	Max gain			15		dB
A_{MAX}	Max attenuation			-15		dB
A_{STEP}	Step resolution		0.5	1	1.5	dB
E_A	Attenuation set error		-0.75	0	+0.75	dB
E_T	Tracking error				2	dB
V_{DC}	DC steps	Adjacent attenuation steps		0.1	3	mV
		From 0 dB to G_{MIN}		0.5	5	mV
Soft mute						
A_{MUTE}	Mute attenuation		80	100		dB
T_D	Delay time	T1		0.48		ms
		T2		0.96		ms
		T3		8		ms
		T4		16		ms
$V_{TH\ Low}$	Low threshold for SM pin				1	V
$V_{TH\ High}$	High threshold for SM pin		2.5			V
R_{PU}	Internal pull-up resistor		32	45	58	kΩ
V_{PU}	Internal pull-up Voltage			3.3		V
Bass control						
Fc	Center frequency	f_{C1}	54	60	66	Hz
		f_{C2}	72	80	88	Hz
		f_{C3}	90	100	110	Hz
		f_{C4}	180	200	220	Hz
Q_{BASS}	Quality factor	Q_1	0.9	1	1.1	
		Q_2	1.1	1.25	1.4	
		Q_3	1.3	1.5	1.7	
		Q_4	1.8	2	2.2	
C_{RANGE}	Control range		±14	±15	±16	dB
A_{STEP}	Step resolution		0.5	1	1.5	dB
DC_{GAIN}	Bass-DC-gain	DC = off	-1	0	+1	dB
		DC = on, Gain = ±15 dB		±4.4		dB

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Middle control						
C_{RANGE}	Control range		±14	±15	±16	dB
A_{STEP}	Step resolution		0.5	1	1.5	dB
f_c	Center frequency	f_{C1}	400	500	600	Hz
		f_{C2}	0.8	1	1.2	kHz
		f_{C3}	1.2	1.5	1.8	kHz
		f_{C4}	2	2.5	3	kHz
Q_{BASS}	Quality factor	Q_1	0.45	0.5	0.55	
		Q_2	0.65	0.75	0.85	
		Q_3	0.9	1	1.1	
		Q_4	1.1	1.25	1.4	
Treble control						
C_{RANGE}	Clipping level		±14	±15	±16	dB
A_{STEP}	Step resolution		0.5	1	1.5	dB
f_c	Center frequency	f_{C1}	8	10	12	kHz
		f_{C2}	10	12.5	15	kHz
		f_{C3}	12	15	18	kHz
		f_{C4}	14	17.5	21	kHz
Speaker attenuators						
A_{MIN}	Min attenuation		-1	0	1	dB
A_{MAX}	Max attenuation		-89	-79	-69	dB
A_{STEP}	Step resolution		0.5	1	1.5	dB
A_{MUTE}	Mute attenuation		80	90		dB
E_E	Attenuation set error				2	dB
V_{DC}	DC steps	Adjacent attenuation steps		0.1	5	mV
Audio outputs						
V_{CL}	Clipping level	d = 0.3%; Byte8_D6=1	2			V_{RMS}
		d = 1%; Byte8_D6=0	2.2			V_{RMS}
R_{OUT}	Output impedance			30	100	Ω
R_L	Output load resistance		2			kΩ
C_L	Output load capacitor				10	nF
V_{DC}	DC voltage level		3.8	4.0	4.2	V
Subwoofer attenuator						
G_{MAX}	Max gain		14	15	16	dB
A_{MAX}	Max attenuation		-83	-79	-75	dB
A_{STEP}	Step resolution		0.5	1	1.5	dB
A_{MUTE}	Mute attenuation		80	90		dB
E_E	Attenuation set error				2	dB

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{DC}	DC steps	Adjacent attenuation steps		0.1	5	mV
Subwoofer lowpass						
f_{LP}	Lowpass corner frequency	f_{LP1}	72	80	88	Hz
		f_{LP2}	108	120	132	Hz
		f_{LP3}	144	160	176	Hz
DC offset detection circuit						
V_{th}	Zero comp window size	V1		±25		mV
		V2		±50		mV
		V3		±75		mV
		V4		±100		mV
t_{sp}	Max rejected spike length			11		µs
				22		µs
				33		µs
				44		µs
$I_{CHDCErr}$	DCErr charge current			5		µA
$I_{DISDCErr}$	DCErr discharge current			5		mA
V_{OutH}	DCErr high volotage			3.3		V
V_{OutH}	DCErr low voltage			100		mV
Level meter						
Vout	Output voltage range		0		3.3	V
V_{LEVEL}	Output level	V_{in} = 1 Vrms		1.6		V
		V_{in} = AC grounded		0		V
T_{DEL}	Analog output delay time			2		µs
General						
e_{NO}	Output noise	BW = 20 Hz to 20 kHz A-Weighted, all gain = 0 dB		12		µV
		BW = 20 Hz - 20 kHz A-Weighted, output muted		6		µV
S/N	Signal to noise ratio	all gain = 0 dB, A-weighted; $V_o = 2\ V_{RMS}$		104		dB
D	Distortion	$V_{IN} = 1\ V_{RMS;}$ all stages 0dB		0.01		%
S_C	Channel separation left/right			90		dB

1. When DC offset detector is not used, the impedance of mono single-ended input is 50 kΩ instead of 100 kΩ.

4 Description

4.1 Input configuration

4.1.1 Front and rear selector

The input stage (Main source and 2nd source) is configurable to adapt to different application. There are 7 different configurations which provide different input structure and different number of input sources as shown below.

- 4 x QD,
- 2 x QD + 3 x SE,
- 1 x QD + 5 x SE,
- 1 x QD + 3 x SE + 2 x MD,
- 3 x QD + 1 x FD,
- 3 x QD + 2 x SE,
- 1 x QD + 2 x SE + 1 x FD + 1 x MD,
- 1 x QD + 3 x SE + 1 x FD

Note: QD = Quasi-Differential, SE = Single-ended input, FD = Full Differential, MD = mono Differential

The configuration of the input stage is controlled by 'Input Configuration' bits in I²C control table (Byte0 Bit5~Bit7). The table below shows the configuration of input pins in different configurations.

Table 6. Input pin configuration

Pin	Pin name	Configuration bits (Byte0 Bit7~Bit5)															
		"000"		"001"		"010"		"011"		"100"		"101"		"110"		"111"	
		CFG0		CFG1		CFG2		CFG3		CFG4		CFG5		CFG6		CFG7	
1	QD1L_SE1L_MD3+	QD1L	IN0	SE1L	IN0	SE1L	IN0	SE1L	IN0	QD1L	IN0	QD1L	IN0	MD3+	IN7	SE1L	IN0
2	QD1R_SE1R_MD3-	QD1R		SE1R		SE1R		SE1R		QD1R		QD1R		MD3-		SE1R	
3	QD1G_SE2L	QD1G		SE2L	IN4	SE2L	IN4	SE2L	IN4	QD1G		QD1G		SE2L	IN4	SE2L	IN4
4	QD2G_SE2R	QD2G	IN1	SE2R		SE2R		SE2R		QD2G	IN1	QD2G	IN1	SE2R		SE2R	
5	QD2L_SE3L	QD2L		SE3L	IN1	SE3L	IN1	SE3L	IN1	QD2L		QD2L		SE3L	IN1	SE3L	IN1
6	QD2R_SE3R	QD2R		SE3R		SE3R		SE3R		QD2R		QD2R		SE3R		SE3R	
7	QD3L	QD3L	IN2	QD3L	IN2	QD3L	IN2	QD3L	IN2	QD3L	IN2	QD3L	IN2	QD3L	IN2	QD3L	IN2
8	QD3G	QD3G		QD3G		QD3G		QD3G		QD3G		QD3G		QD3G		QD3G	
9	QD3R	QD3R		QD3R		QD3R		QD3R		QD3R		QD3R		QD3R		QD3R	
10	QD4L_FD4+_SE4L_MD1+	QD4L	IN3	QD4L	IN3	SE4L	IN5	MD1+	IN3	FD4L+	IN3	SE4L	IN5	FD4L+	IN3	FD4L+	IN3
11	QD4G_FD4L_SE4R_MD1-	QD4G		QD4G		SE4R		MD1-		FD4L-		SE4R		FD4L-		FD4L-	
12	QD4G_FD4R_SE5L_MD2-	QD4G		QD4G		SE5L	IN6	MD2-	IN3	FD4R-		SE5L	IN6	FD4R-		FD4R-	
13	QD4R_FD4R+_SE5R_MD2+	QD4R		QD4R		SE5R		MD2+		FD4R+		SE5R		FD4R+		FD4R+	

With different input configuration, the input source can be selected with input selector (Byte0/1 Bit0~Bit2). The following matrix defines the selector configuration of different input sources dependant on the configuration bits.

Table 7. Selector configuration matrix

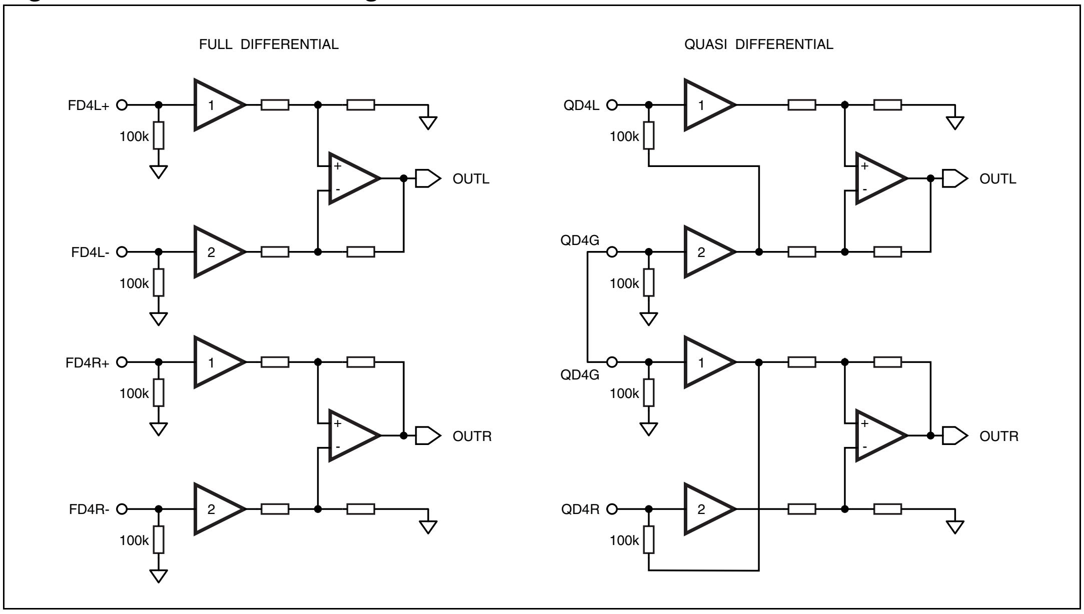
Selector Bits (Byte0/1 Bit2~Bit0)	000	001	010	011	100	101	110	111
	IN0	**IN1**	**IN2**	**IN3**	**IN4**	**IN5**	**IN6**	**IN7**
CFG0	QD1	QD2	QD3	QD4	NA	NA	NA	NA
CFG1	SE1	SE3	QD3	QD4	SE2	NA	NA	NA
CFG2	SE1	SE3	QD3	NA	SE2	SE4	SE5	NA
CFG3	SE1	SE3	QD3	MD1/2	SE2	NA	NA	NA
CFG4	QD1	QD2	QD3	FD	NA	NA	NA	NA
CFG5	QD1	QD2	QD3	NA	NA	SE4	SE5	NA
CFG6	NA	SE3	QD3	FD	SE2	NA	NA	MD3
CFG7	SE1	SE3	QD3	FD	SE2	NA	NA	NA

Note: *In each configuration, only the light grey cells are allowed. The dark grey cells are not allowed.*
MD1/MD2 selection is defined by extra bit – 'MD1/2 selection' in I^2C control table (Bit3 of Byte0/1).

The input stage can be configured to 0dB or 3dB gain with I^2C bus. The 0dB configuration allows up to 2Vrms input signal level, while with 3dB gain, the internal signal will start to clip when input signal level is higher than 1.414Vrms.

The Pin10~Pin13 can be configured as full differential input stage or quasi-differential input. When it is configured as quasi-differential input, both Pin11 and Pin12 are used as the QD common input pins. These two pins must be connected together externally in application. In this case the input impedance of QD4 common is reduced to 50kΩ (half of QD4 left and right input). The diagram below shows both QD and FD configuration of QD4/FD4.

Figure 3. QD and FD configuration of QD4/FD4



4.1.2 Direct path

The input pins can be configured as direct path mode by setting Byte1 Bit5~Bit7. In direct path mode the input pins are connected to dedicated mono fader directly, all the filters and volume are bypassed. Below is described the assignment of the input pins and output fader in direct path mode:

Pin5/QD2L --> OUTLF

Pin6/QD2R --> OUTRF

Pin7/QD3L --> OUTLR

Pin9/QD3R --> OUTRR

Pin10/FDL+_QD4L --> OUTL2

Pin13/FDR+_QD4R--> OUTR2

Note: 1 *The configurations CFG2, CFG3 and CFG5 are not recommended in direct path mode. Because in these 3 configurations SE4L/MD1+ and SE5R/MD2+ are connected to OUT2_L and OUT2_R fader separately. In this case left and right channel of OUT2 belongs to different input sources.*

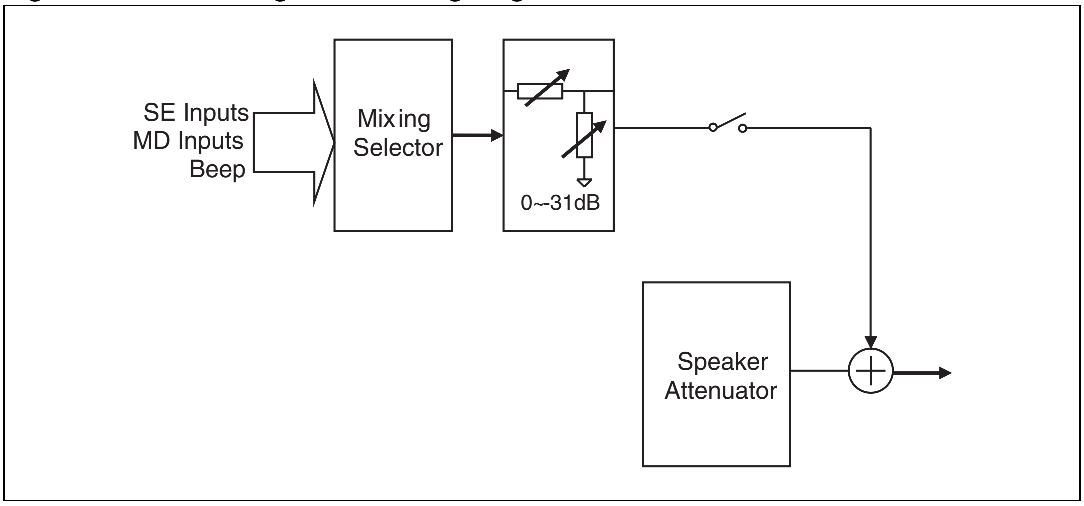
2 *If the direct path is chosen, the input pins have to be used as single ended pins. In case of differential inputs the ground or minus pins must be connect to GND by AC short.*

3 *Inputs in direct path mode are also selectable with front and rear selector.*

4.2 Mixing

The device provides mixing function which allows the mixing source mixed into front and rear speaker output independently. The mixing source can be any single-ended input, mono-differential input or beep input (Mono single-ended input when DC offset detector is not used). In order to adjust the level of mixing signal, the mixing selector is followed with a 0 dB~-31 dB attenuator. The maximum mixing input signal level is 1.6 Vrms for single-ended input and mono-differential input. For beep input, the maximum input signal level is about 1.4 Vrms. The block diagram of the mixing function is shown below.

Figure 4. Block diagram of mixing stage



Since the input stage of this device has different configurations, the corresponding sources for mixing selector are also different according to the configurations. The following table defines the available sources for mixing under different configurations.

Table 8. Available sources for mixing

Mix selector bits (Byte2 Bit2~Bit0)	000	001	010	011	100	101	110	111
	MixIN0	MixIN1	MixIN2	MixIN3	MixIN4	MixIN5	MixIN6	MixIN7
CFG0	NA	NA	NA	NA	NA	NA	Beep	Mute
CFG1	SE1	SE2	SE3	NA	NA	NA	Beep	Mute
CFG2	SE1	SE2	SE3	SE4	SE5	NA	Beep	Mute
CFG3	SE1	SE2	SE3	MD1	NA	MD2	Beep	Mute
CFG4	NA	NA	NA	NA	NA	NA	Beep	Mute
CFG5	NA	NA	NA	SE4	SE5	NA	Beep	Mute
CFG6	MD3	SE2	SE3	NA	NA	NA	Beep	Mute
CFG7	SE1	SE2	SE3	NA	NA	NA	Beep	Mute

Note: Only light grey cells are allowed mixing input. The dark grey cells are not allowed.
The beep input is available only when DC offset detector function is not used.

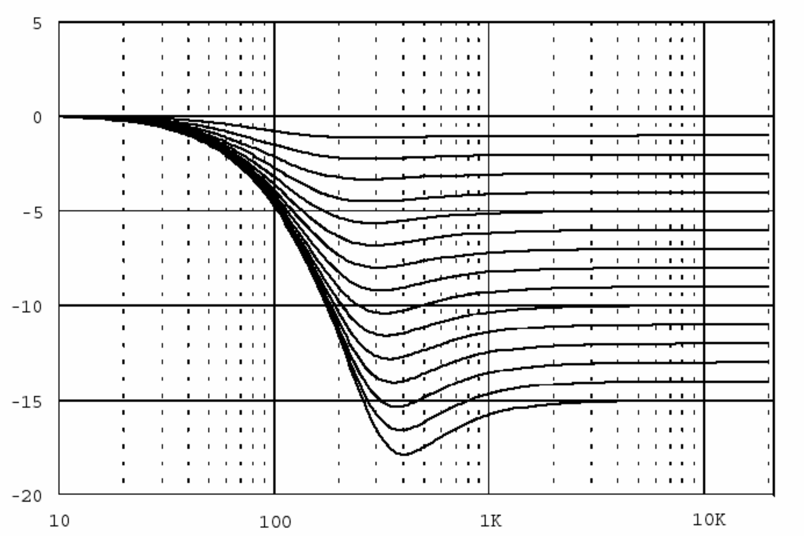
4.3 Loudness

There are four parameters programmable in the loudness stage:

4.3.1 Loudness attenuation

Figure 5 shows the attenuation as a function of frequency at f_P = 400 Hz

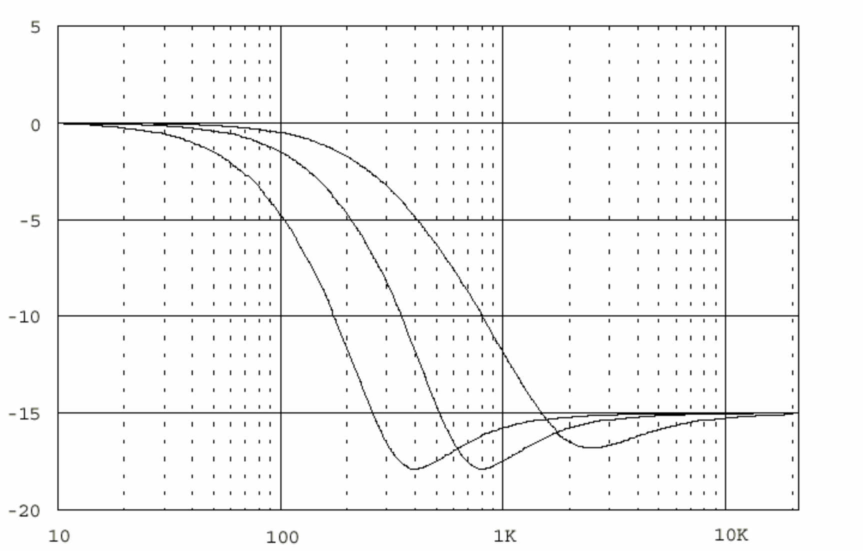
Figure 5. Loudness attenuation @ f_P = 400 Hz.



4.3.2 Peak frequency

Figure 6 shows the four possible peak-frequencies at 400, 800 and 2400 Hz

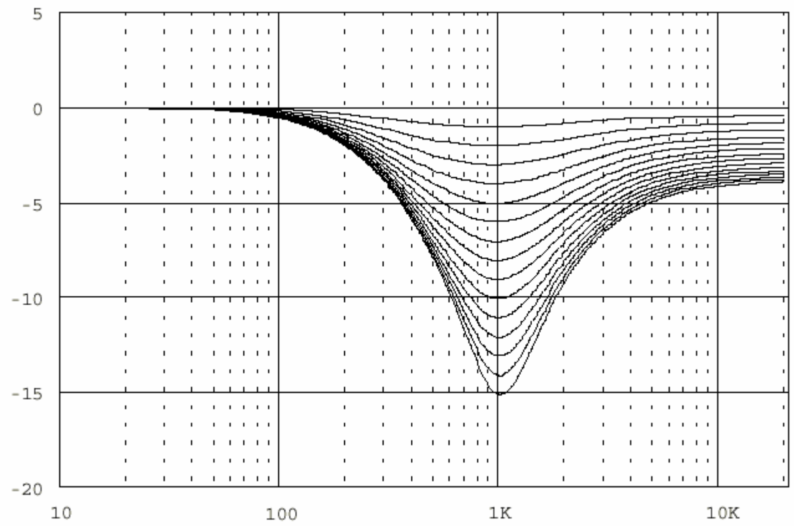
Figure 6. Loudness center frequencies @ Attn. = 15 dB.



4.3.3 High frequency boost

Figure 7 shows the different Loudness shapes in low and high frequency boost.

Figure 7. Loudness attenuation, f_c =2.4 kHz



4.3.4 Flat mode

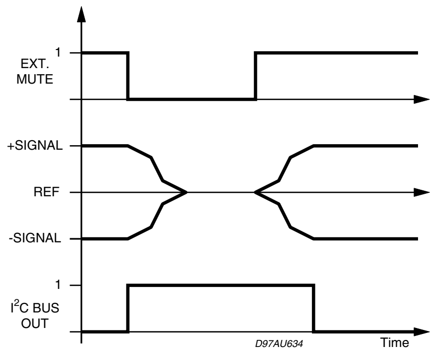
In flat mode the loudness stage works as a 0dB to -15dB attenuator.

4.4 SoftMute

The digitally controlled SoftMute stage allows muting/demuting the signal with a I^2C-bus programmable slope. The mute process can either be activated by the SoftMute pin or by the I^2C-bus. This slope is realized in a special S-shaped curve to mute slow in the critical regions (see *Figure 8*).

For timing purposes the Bit0 of the I^2C-bus output register is set to 1 from the start of muting until the end of demuting.

Figure 8. SoftMute timing



1. A started Mute action is always terminated and could not be interrupted by a change of the mute signal.

4.5 Softstep volume

When the volume-level is changed audible clicks could appear at the output. The root cause of those clicks could either be a DC Offset before the volume-stage or the sudden change of the envelope of the audio signal. With the Softstep feature both kinds of clicks could be reduced to a minimum and are no more audible. The blend-time from one step to the next is programmable as 5 ms or 10 ms. The softstep control is described in detail in *Chapter 4.10*.

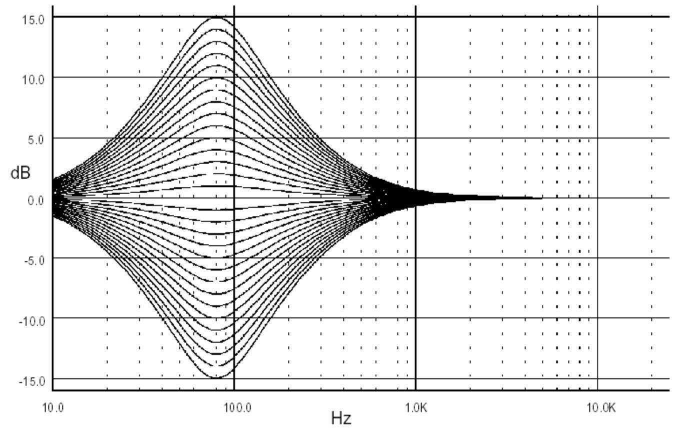
4.6 Bass

There are four parameters programmable in the bass stage:

4.6.1 Bass attenuation

Figure 9 shows the attenuation as a function of frequency at a center frequency of 80 Hz.

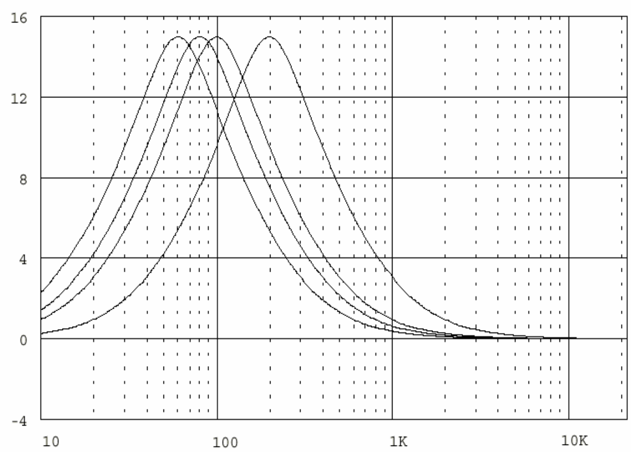
Figure 9. Bass Control @ f_c = 80 Hz, Q = 1



4.6.2 Bass center frequency

Figure 10 shows the four possible center frequencies 60, 80, 100 and 200 Hz.

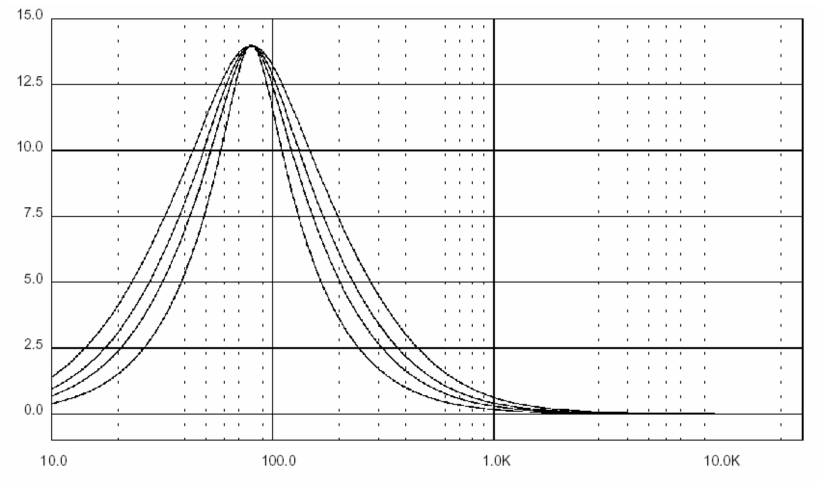
Figure 10. Bass center frequencies @ gain = 14 dB, Q = 1



4.6.3 Bass quality factors

Figure 11 shows the four possible quality factors 1, 1.25, 1.5 and 2.

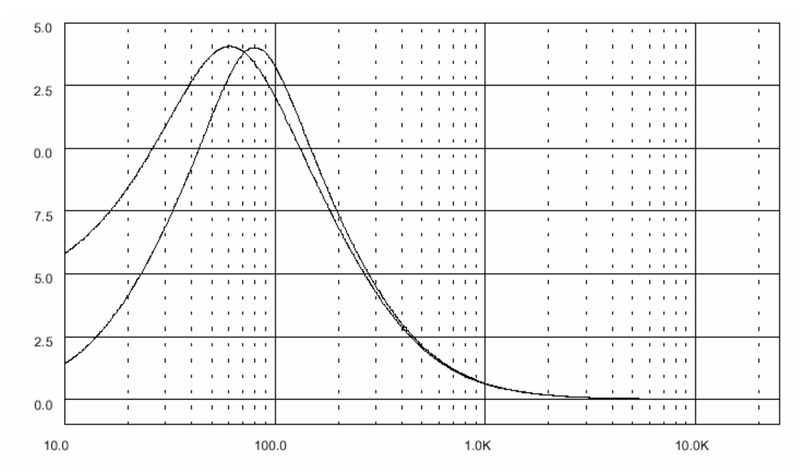
Figure 11. Bass quality factors @ gain = 14 dB, f_c = 80 Hz



4.6.4 DC mode

In this mode the DC gain is increased by 4.4 dB. In addition the programmed center frequency and quality factor is decreased by 25 % which can be used to reach alternative center frequencies or quality factors.

Figure 12. Bass normal and DC mode @ Gain = 14 dB, f_c = 80 Hz



1. The center frequency, Q and DC-mode can be set fully independently.

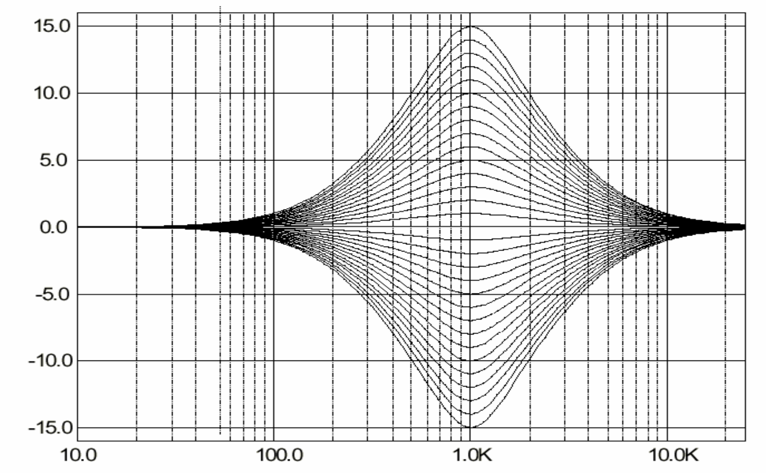
4.7 Middle

There are three parameters programmable in the middle stage:

4.7.1 Middle attenuation

Figure 13 shows the attenuation as a function of frequency at a center frequency of 1 kHz.

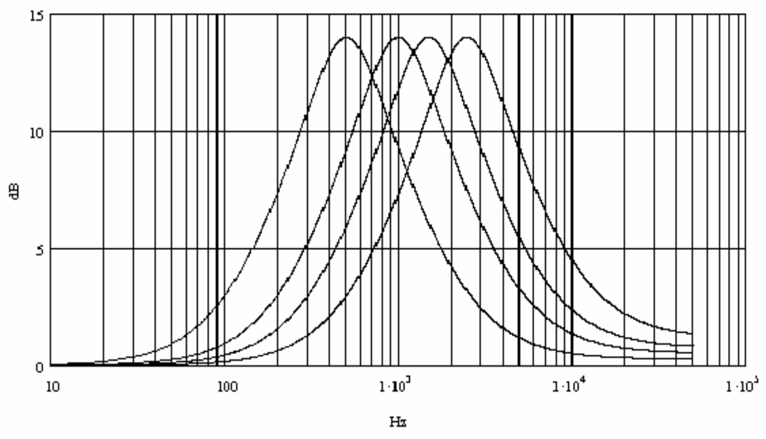
Figure 13. Middle control @ f_c = 1 kHz, Q = 1



4.7.2 Middle center frequency

Figure 14 shows the four possible center frequencies 500 Hz, 1 kHz, 1.5 kHz and 2.5 kHz.

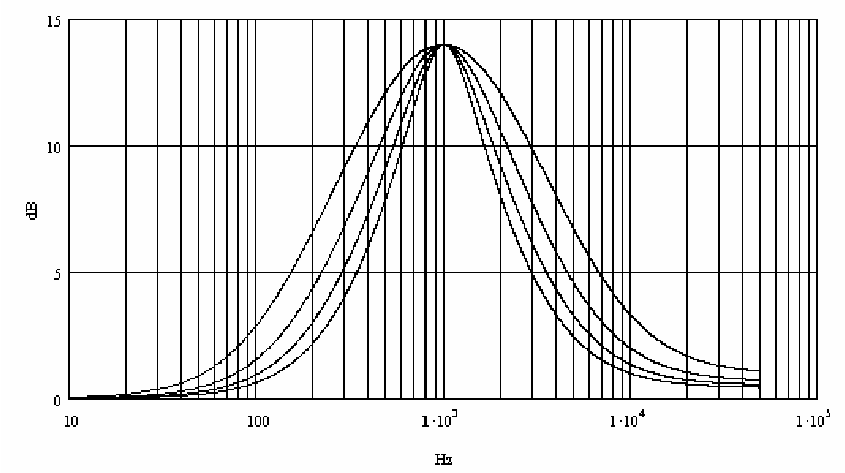
Figure 14. Middle center frequencies @ gain = 14d B, Q = 1



4.7.3 Middle quality factors

Figure 15 shows the four possible quality factors 0.5, 0.75, 1 and 1.25.

Figure 15. Middle quality factors @ gain = 14 dB, f_c = 1 kHz



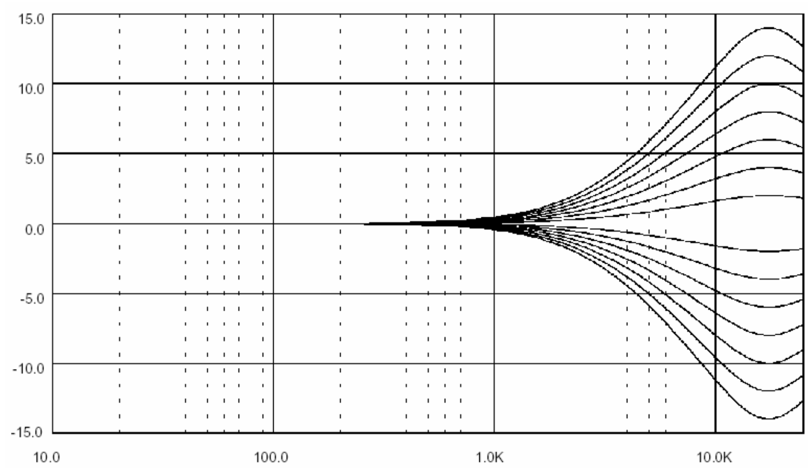
4.8 Treble

There are two parameters programmable in the treble stage:

4.8.1 Treble attenuation

Figure 16 shows the attenuation as a function of frequency at a center frequency of 17.5 kHz.

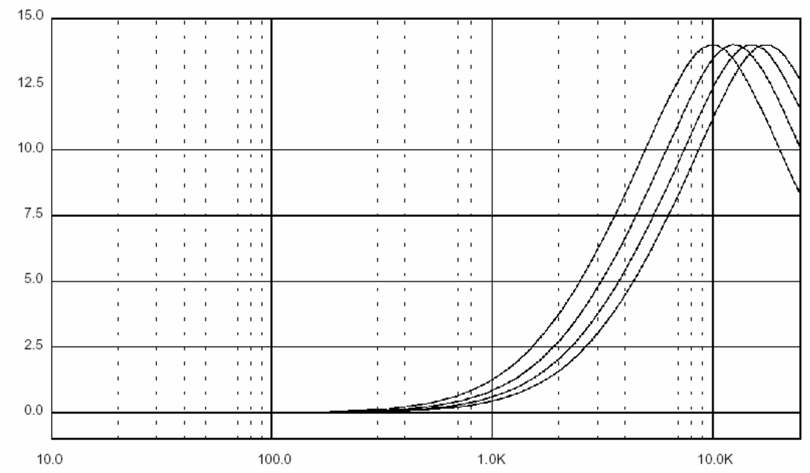
Figure 16. Treble Control @ f_c = 17.5 kHz.



4.8.2 Treble center frequency

Figure 17 shows the four possible center frequencies 10 k, 12.5 k, 15 k and 17.5 kHz.

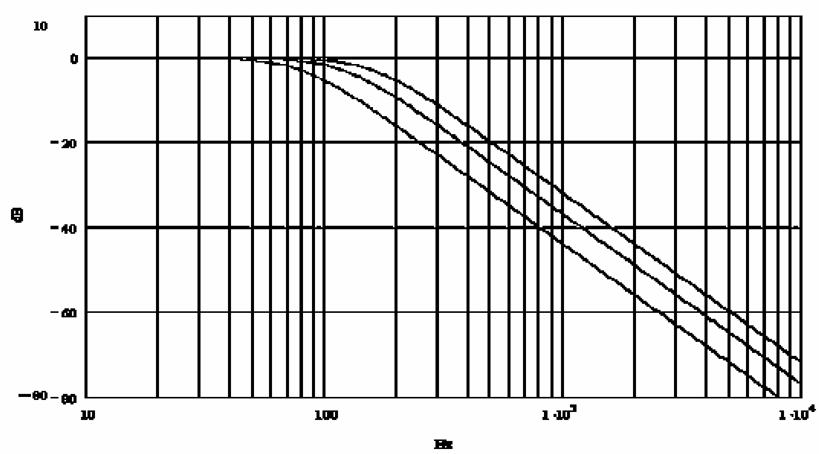
Figure 17. Treble center frequencies @ gain = 14 dB



4.9 Subwoofer Filter

The subwoofer lowpass filter has Butterworth characteristics with programmable cut-off frequency (80 / 120 / 160 Hz). The output phase can be selected between 0 deg and 180 deg. The input of subwoofer takes signal from bass filter output or output of input mux.

Figure 18. Subwoofer control



4.10 Softstep control

In this device, the softstep function is available for volume, speaker, loudness, treble, middle and bass block. With softstep function, the audible noise of DC offset or the sudden change of signal can be avoided when adjusting gain setting of the block.

For each block, the softstep function is controlled by softstep on/off control bit in the control table. The softstep transient time selection (5 ms or 10 ms) is common for all blocks and it is controlled by softstep time control bit. The softstep operation of all blocks has a common centralized control. In this case, a new softstep operation can not be started before the completion previous softstep.

There are two different modes to activate the softstep operation. The softstep operation can be started right after I^2C data sending, or the softstep can be activated in parallel after data sending of several different blocks. The two modes are controlled by the 'act bit' (it is normally bit7 of the byte.) of each byte. When act bit is '0', which means action, the softstep is activated right after the date byte is sent. When the act bit is '1', which means wait, the block goes to wait for softstep status. In this case, the block will wait for some other block to activate the operation. The softstep operation of all blocks in wait status will be done together with the block which activate the softstep. With this mode, all specific blocks can do the softstep in parallel. This avoids waiting when the softstep is operated one by one.

Chip Addr	Sub Addr	0xxxxxxx

|↑ Softstep start here

Chip Addr	Sub Addr	1xxxxxxx	1xxxxxxx	......	0xxxxxxx

|↑ Softstep start here for all

1. It is not allowed to cross 0 dB with softstep directly. From plus gain to minus gain, it must go to +0 dB first, then destination. From minus gain to plus gain, it must go to -0 dB first, and then destination.
2. When one block is in 'wait for softstep' status, it is not allowed to send data to this block again before its softstep is completed.
3. To know if there is a softstep in operation, it is possible to monitor the 'busy' signal by I^2C transmission mode (*Section 5.1.2*). When softstep is busy (busy=0), it is better to wait before sending new data until it is free (busy=1).

4.11 DC offset detector and level meter option

This device provide DC offset detector function and level meter function option. In one specific application, only one of the function can be used. The configuration of the function is controlled by I^2C bus (Byte3 Bit7).

When the device uses DC offset detector function, Pin22, Pin27 and Pin28 are used as WinTC, DCErr and WinIN for DC offset detector. When it is configured as level meter, DCErr becomes level meter output. In the mean time, WinIN is used as beep input (Mono single-ended input for mixing), and WinTC becomes a reference voltage output (4 V external DC voltage or 3.3 V internal reference voltage).

4.12 DC offset detector

Using the DC offset detection circuit (*Figure 19*) an offset voltage difference between the audio power amplifier and the TDA7719's Front and Rear outputs can be detected, preventing serious damage to the loudspeakers. The circuit compares whether the signal crosses the zero level inside the audio power at the same time as in the speaker cell. The output of the zero-window-comparator of the power amplifier must be connected with the WinIn-input of the TDA7719. The WinIn-input has an internal pull-up resistor connected to 5.5Volts. It is recommended to drive this pin with open-collector outputs only.

To compensate for errors at low frequencies the WinTC-pin are implemented, with external capacitors introducing the same delay $\tau = 7.5k\Omega * C_{ext}$ as the AC-coupling between the TDA7719 and the power amplifier introduces. For the zero window comparators, the time constant for spike rejection as well as the threshold are programmable.

For electrical characteristics see *Chapter 3 on page 9*.

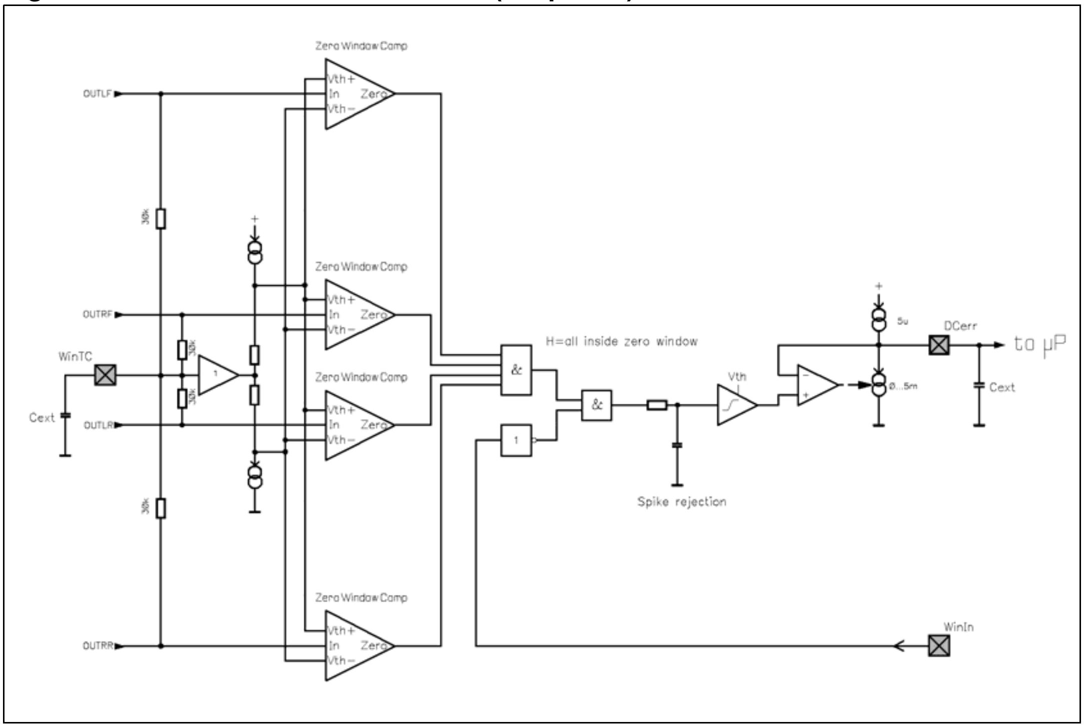
A low-active DC-offset error signal appears at the DCErr output if the next conditions are both true:

a) Front and rear outputs are inside zero crossing windows.

b) The Input voltage VWinIn is logic low whenever at least one output of the power amplifier is outside the zero crossing windows.

After power-on, the external attached capacitor is rapidly charged (fast-charge) to overcome a false indication.

Figure 19. DC offset detection circuit (simplified)



4.13 Level meter

In case of not using DC offset detector, the three pins used for DCO can be configured as other function. Pin27 (DC_Err / LMOUT) becomes the level meter output. The level meter block takes signal after main input selector and mix signal into mono, then rectify the signal and detect the peak of the signal. The output stage of level meter removes the DC voltage of the signal and the output voltage level shows exactly the Vpeak of signal. Since the discharge time constant of the level meter is quite slow, it is necessary to reset level meter regularly (with I^2C bus control Byte3 Bit6) to get correct peak information of the signal.

4.14 Output gain control

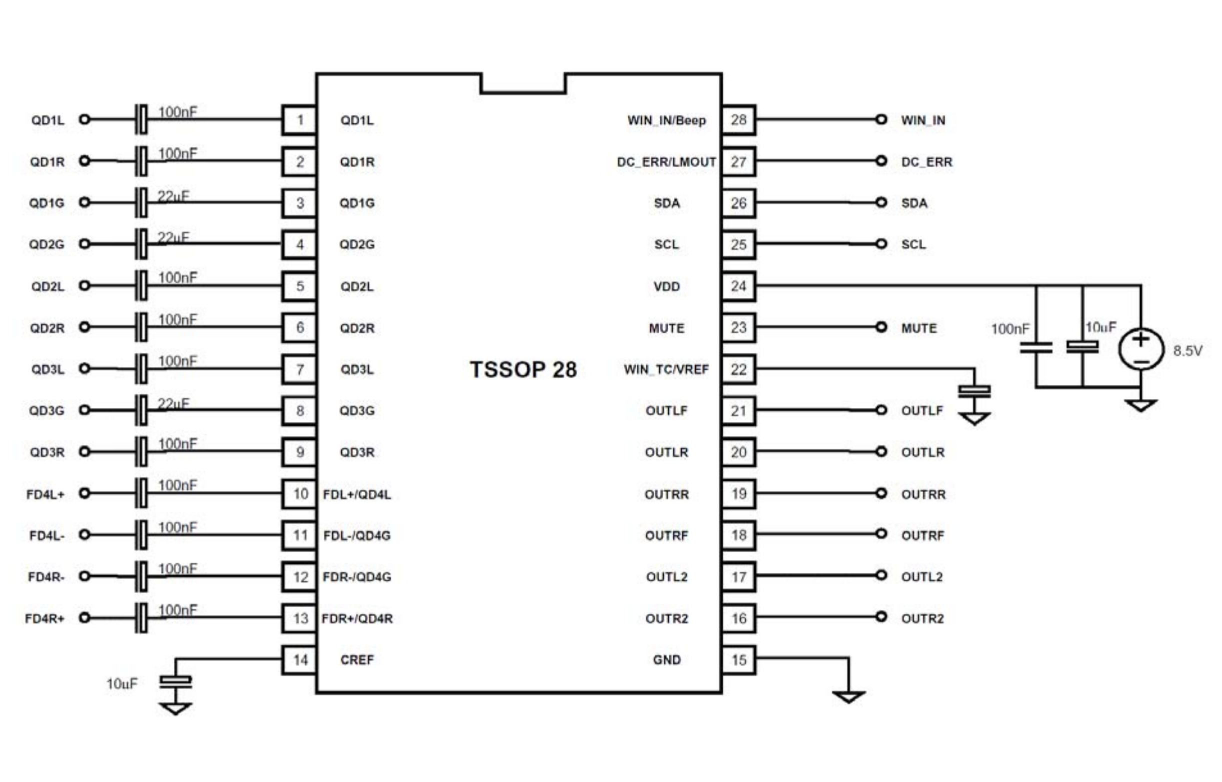
The output stage of the device can provide a option to have additional 1 dB gain in order to boost the maximum output level to 2.2 Vrms with maximum 1 % distortion.

4.15 Audioprocessor testing

In the test mode, which can be activated by setting bit D7 of the I^2C subaddress byte and bit D0 of the testing-audioprocessor byte, several internal signals are available at the QD1L pin. In this mode, the input resistance of 100 kΩ is disconnected from the pin. Internal signals available for testing are listed in the data-byte specification.

4.16 Test circuit (3 x QD + 1 x FD + DC offset detector)

Figure 20. Test circuit

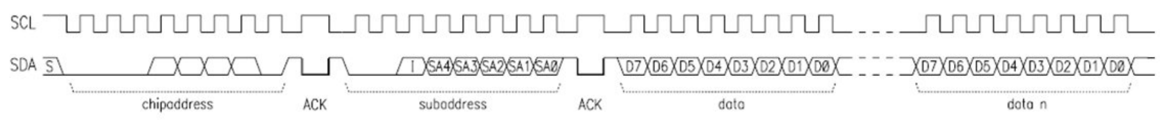


5 I²C bus specification

5.1 Interface protocol

The interface protocol comprises:
- a start condition (S)
- a chip address byte (the LSB determines read/write transmission)
- a subaddress byte
- a sequence of data (N-bytes + acknowledge)
- a stop condition (P)
- the max. clock speed is 400 kbits/s
- 3.3 V logic compatible

Figure 21. Switching characteristics

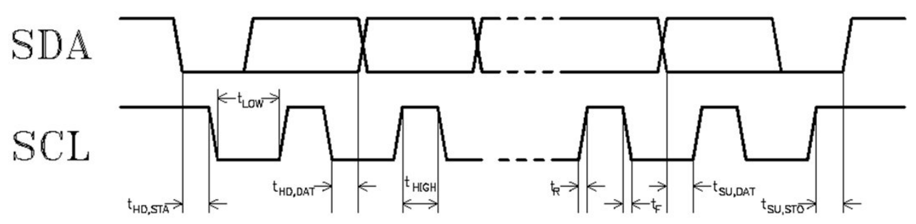


S = Start
ACK = Acknowledge

Table 9. I²C bus electrical characterisitics

Symbol	Parameter	Min	Max	Unit
f_{SCL}	SCL clock frequency		400	kHz
V_{IH}	High level input voltage	2.4		V
V_{IL}	Low level input voltage		0.8	V
$t_{HD,STA}$	Hold time for START	0.6		µs
$t_{SU,STO}$	Setup time for STOP	0.6		µs
t_{LOW}	Low period for SCL clock	1.3		µs
t_{HIGH}	High period for SCL clock	0.6		µs
t_F	Fall time for SCL/SDA		300	ns
t_R	Rise time for SCL/SDA		300	ns
$t_{HD,DAT}$	Data hold time	0		ns
$t_{SU,DAT}$	Data setup time	100		ns

Figure 22. I²C timing diagram



5.1.1 Receive mode

S	1	0	0	0	1	0	0	R/W	ACK	TS	X	AI	A4	A3	A2	A1	A0	ACK	DATA	ACK	P

S = Start

R/W = "0" -> Receive Mode (Chip can be programmed by µP)

"1" -> Transmission Mode (Data could be received by µP)

ACK = Acknowledge

P = Stop

TS = Testing mode

AI = Auto increment

5.1.2 Transmission mode

S	1	0	0	0	1	0	0	R/W	ACK	X	X	X	X	X	X	BZ	SM	ACK	P

SM = Soft mute activated for main channel

BZ = Softstep Busy ('0' = Busy)

X = Not used

The transmitted data is automatic updated after each ACK. Transmission can be repeated without new chip address.

5.1.3 Reset condition

A Power-On-Reset is invoked if the supply voltage is below than 3.5V. After that the registers are initialized to the default data written in following tables.

Table 10. Subaddress (receive mode)

MSB							LSB	Function
I2	I1	I0	A4	A3	A2	A1	A0	
								Testing Mode
0								Off
1								On
	x							**Not used**
								Auto Increment Mode
		0						Off
		1						On
			0	0	0	0	0	Input Configuration / Main Source Selector
			0	0	0	0	1	2nd Source Selector / Direct Path
			0	0	0	1	0	Mixing Source / Mixing Gain
			0	0	0	1	1	Mix Control / Level Meter / DC Offset Detector Config
			0	0	1	0	0	Soft Mute / Others
			0	0	1	0	1	Soft Step I
			0	0	1	1	0	Soft Step II / DC-detector
			0	0	1	1	1	Loudness
			0	1	0	0	0	Volume / Output Gain
			0	1	0	0	1	Treble
			0	1	0	1	0	Middle
			0	1	0	1	1	Bass
			0	1	1	0	0	Subwoofer / Middle / Bass
			0	1	1	0	1	Speaker Attenuator Left Front
			0	1	1	1	0	Speaker Attenuator Right Front
			0	1	1	1	1	Speaker Attenuator Left Rear
			1	0	0	0	0	Speaker Attenuator Right Rear
			1	0	0	0	1	Subwoofer Attenuator Left
			1	0	0	1	0	Subwoofer Attenuator Right
			1	0	0	1	1	Testing Audio Processor 1
			1	0	1	0	0	Testing Audio Processor 2

5.2 Data byte specification

The default power on status of the registers is written with underline.

Table 11. Input configuration / main selector (0)

MSB							LSB	Function
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
								Main source selector
					0	0	0	IN0
					0	0	1	IN1
					0	1	0	<u>IN2</u>
					0	1	1	IN3
					1	0	0	IN4
					1	0	1	IN5
					1	1	0	IN6
					1	1	1	IN7
								MD1/2 configuration for main selector
				0				MD1
				1				<u>MD2</u>
								Main source input gain select
			0					0dB
			1					<u>3dB</u>
								Input configuration
0	0	0						CFG0
0	0	1						CFG1
0	1	0						CFG2
0	1	1						CFG3
1	0	0						CFG4
1	0	1						CFG5
1	1	0						CFG6
1	1	1						<u>CFG7</u>

Note: For detailed input source and input stage configuration, please refer to Section 4.1.

Table 12. 2nd Source selector / direct path (1)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								2nd Source Selector
					0	0	0	IN0
					0	0	1	IN1
					0	1	0	IN2
					0	1	1	IN3
					1	0	0	IN4
					1	0	1	IN5
					1	1	0	IN6
					1	1	1	IN7
								MD1/2 Configuration for 2nd Selector
				0				MD1
				1				MD2
								2nd Source Input Gain Select
			0					0dB
			1					3dB
								QD2 Bypass (Front)
		0						on
		1						Off
								QD3 Bypass (Rear)
	0							on
	1							Off
								QD4 Bypass (Subwoofer)
0								on
1								Off

Note: For detailed input source and input stage configuration, please refer to Section 4.1.

To active QD3 Bypass (Rear) function, it needs to set Byte3_D4 to "Direct Path / 2nd Source" also.

Table 13. Mixing source / mixing gain (2)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Mixing Source Selector
					0	0	0	IN0
					0	0	1	IN1
					0	1	0	IN2
					0	1	1	IN3
					1	0	0	IN4
					1	0	1	IN5
					1	1	0	IN6
					1	1	1	IN7
								Mixing Attenuator
0	0	0	0	0				0dB
0	0	0	0	1				-1dB
0	0	0	1	0				-2dB
0	0	0	1	1				-3dB
0	0	1	0	0				-4dB
0	0	1	0	1				-5dB
0	0	1	1	0				-6dB
0	0	1	1	1				-7dB
0	1	0	0	0				-8dB
0	1	0	0	1				-9dB
0	1	0	1	0				-10dB
0	1	0	1	1				-11dB
0	1	1	0	0				-12dB
0	1	1	0	1				-13dB
0	1	1	1	0				-14dB
0	1	1	1	1				-15dB
1	0	0	0	0				-16dB
1	0	0	0	1				-17dB
1	0	0	1	0				-18dB
1	0	0	1	1				-19dB
1	0	1	0	0				-20dB
1	0	1	0	1				-21dB
1	0	1	1	0				-22dB
1	0	1	1	1				-23dB
1	1	0	0	0				-24dB
1	1	0	0	1				-25dB
1	1	0	1	0				-26dB
1	1	0	1	1				-27dB
1	1	1	0	0				-28dB
1	1	1	0	1				-29dB
1	1	1	1	0				-30dB
1	1	1	1	1				-31dB

Table 14. Mix control / level meter / dc offset detector configure (3)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Mix to Front Left
							0	On
							1	Off
								Mix to Front Right
						0		On
						1		Off
								Mix to Rear Left
					0			On
					1			Off
								Mix to Rear Right
				0				On
				1				Off
								Rear Speaker Input Configuration
			0					Direct Path / 2nd Source
			1					Main Signal
								Reference Output Select
		0						Internal Vref (3.3V)
		1						External Vref (4V)
								Level Meter Reset
	0							Normal
	1							Reset
								DC Offset Detector / Level Meter Config
0								Level Meter
1								DC Offset Detector

Table 15. Soft mute / others (4)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
							0 1	**Soft Mute** On Off
						0 1		**Pin Influence for Mute** Pin and IIC IIC
				0 0 1 1	0 1 0 1			**Soft Mute Time** 0.48ms 0.96ms 7.68ms 15.36ms
			0 1					**Subwoofer Input Configuration** Input Mux Bass Output
		0 1						**Subwoofer Enable (OUTL3 & OUTR3)** On Off
	0 1							**Fast Charge** On Off
0 1								**Anti-Alias Filter** On Off (bypass)

Table 16. SoftStep I (5)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Loudness Soft Step
							0	On
							1	Off
								Volume Soft Step
						0		On
						1		Off
								Treble Soft Step
					0			On
					1			Off
								Middle Soft Step
				0				On
				1				Off
								Bass Soft Step
			0					On
			1					Off
								Speaker LF Soft Step
		0						On
		1						Off
								Speaker RF Soft Step
	0							On
	1							Off
								Speaker LR Soft Step
0								On
1								Off

Table 17. SoftStep II / DC detector (6)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Speaker RR Soft Step
							0	on
							1	off
								Subwoofer Left Soft Step
						0		on
						1		off
								Subwoofer Right Soft Step
					0			on
					1			off
								Soft Step Time
				0				5ms
				1				10ms
								Zero-comparator Window size
		0	0					±100mV
		0	1					±75mV
		1	0					±50mV
								Spike rejection time constant
0	0							11µs
0	1							22 µs
1	0							33 µs
1	1							44 µs

Table 18. Loudness (7)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
				 0 0 : 1 1	 0 0 : 1 1	 0 0 : 1 1	 0 1 : 0 1	**Attenuation** 0dB -1dB : -14dB -15dB
		 0 0 1 1	 0 1 0 1					**Center Frequency** Flat 400Hz 800Hz 2400Hz
	 0 1							**High Boost** on off
 0 1								**Soft Step Action** act wait

Table 19. Volume / output gain (8)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
			 0 0 : 0 0 1 1 : 1 1	 0 0 : 1 1 1 1 : 0 0	 0 0 : 1 1 1 1 : 0 0	 0 0 : 1 1 1 1 : 0 0	 0 1 : 0 1 1 0 : 1 0	**Gain/Attenuation** -15dB -14dB : -1dB 0dB 0dB +1dB : +14dB +15dB
		x						**Not used**
	 0 1							**Output Gain** 1dB 0dB
 0 1								**Soft Step Action** act wait

Table 20. Treble filter (9)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Gain/Attenuation
			0	0	0	0	0	-15dB
			0	0	0	0	1	-14dB
			:	:	:	:	:	:
			0	1	1	1	0	-1dB
			0	1	1	1	1	0dB
			1	1	1	1	1	0dB
			1	1	1	1	0	+1dB
			:	:	:	:	:	:
			1	0	0	0	1	+14dB
			1	0	0	0	0	+15dB
								Treble Center Frequency
	0	0						10.0kHz
	0	1						12.5kHz
	1	0						15.0kHz
	1	1						17.5kHz
								Soft Step Action
0								act
1								wait

Table 21. Middle filter (10)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Gain/Attenuation
			0	0	0	0	0	-15dB
			0	0	0	0	1	-14dB
			:	:	:	:	:	:
			0	1	1	1	0	-1dB
			0	1	1	1	1	0dB
			1	1	1	1	1	0dB
			1	1	1	1	0	+1dB
			:	:	:	:	:	:
			1	0	0	0	1	+14dB
			1	0	0	0	0	+15dB
								Middle Q Factor
	0	0						0.5
	0	1						0.75
	1	0						1
	1	1						1.25
								Soft Step Action
0								act
1								wait

Table 22. Bass filter (11)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Gain/Attenuation
			0	0	0	0	0	-15dB
			0	0	0	0	1	-14dB
			:	:	:	:	:	:
			0	1	1	1	0	-1dB
			0	1	1	1	1	0dB
			1	1	1	1	1	0dB
			1	1	1	1	0	+1dB
			:	:	:	:	:	:
			1	0	0	0	1	+14dB
			1	0	0	0	0	+15dB
								Bass Q Factor
	0	0						1.0
	0	1						1.25
	1	0						1.5
	1	1						2.0
								Soft Step Action
0								act
1								wait

Table 23. Subwoofer / middle / bass (12)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Subwoofer Cut-off Frequency
						0	0	flat
						0	1	80Hz
						1	0	120Hz
						1	1	160Hz
								Subwoofer Output Phase
					0			180 deg
					1			0 deg
								Middle Center Frequency
			0	0				500Hz
			0	1				1000Hz
			1	0				1500Hz
			1	1				2500Hz
								Bass Center Frequency
	0	0						60Hz
	0	1						80Hz
	1	0						100Hz
	1	1						200Hz
								Bass DC Mode
0								on
1								off

Table 24. Speaker attenuation (LF/RF/LR/RR) (13-16)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Gain/Attenuation
	0	0	0	0	0	0	0	0dB
	0	0	0	0	0	0	1	0dB
	:	:	:	:	:	:	:	:
	0	0	0	1	1	1	1	0dB
	0	0	1	0	0	0	0	0dB
	0	0	1	0	0	0	1	-1dB
	:	:	:	:	:	:	:	:
	1	0	1	1	1	1	0	-78dB
	1	0	1	1	1	1	1	-79dB
	1	1	x	x	x	x	x	mute
								Soft Step Action
0								act
1								wait

Table 25. Subwoofer attenuation (subwoofer L/subwoofer R) (17-18)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Gain/Attenuation
	0	0	0	0	0	0	0	+0dB
	0	0	0	0	0	0	1	+1dB
	:	:	:	:	:	:	:	:
	0	0	0	1	1	1	1	+15dB
	0	0	1	0	0	0	0	-0dB
	0	0	1	0	0	0	1	-1dB
	:	:	:	:	:	:	:	:
	1	0	1	1	1	1	0	-78dB
	1	0	1	1	1	1	1	-79dB
	1	1	x	x	x	x	x	mute
								Soft Step Action
0								act
1								wait

Table 26. Testing audio processor 1 (19)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Audio Processor Testing Mode
							0	off
							1	on
								Test Multiplexer at QD1L (1)
			0	0	0	0		DCDet Vth High
			0	0	0	1		DCDet Vth Low
			0	0	1	0		VolumeoutL
			0	0	1	1		IntZeroErr
			0	1	0	0		InGainL
			0	1	0	1		LoudoutL
			0	1	1	0		BassoutL
			0	1	1	1		MidoutL
			1	0	0	0		Ref5V5
			1	0	0	1		VGB1.26
			1	0	1	0		SMCLK
			1	0	1	1		TrebleoutL
			1	1	0	0		SSCLK
			1	1	0	1		Clock200k
			1	1	1	0		REQ
			1	1	1	1		SDCLK
								Clock Fast Mode (2)
		0						on
		1						Off
								Clock Source (2)
	0							external (at mute pin)
	1							Internal (200kHz)
x								**Not Used**

1. The control bit needs both I2C test mode on & sub-address test mode on.
2. The control bit does not depend on test mode.

Table 27. Testing audio processor 2 (20)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Test Architecture (1)
							0	normal
							1	Split
								Oscillator Clock (2)
						0		400kHz
						1		800kHz
								Softstep Curve (2)
					0			S-Curve
					1			Linear Curve
								Manual Set Busy Signal (1)
			0	0				Auto
			0	1				Auto
			1	0				0
			1	1				1
								Request for Clk Generator (1)
			0	0				Allow
			0	1				Allow
			1	0				Stopped
			1	1				Stopped
x	x	x						**Not Used**

1. The control bit needs sub-address test mode on
2. The control bit does not depend on test mode.

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

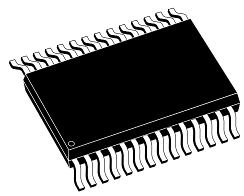
ECOPACK® is an ST trademark.

Figure 23. TSSOP28 mechanical data and package dimensions

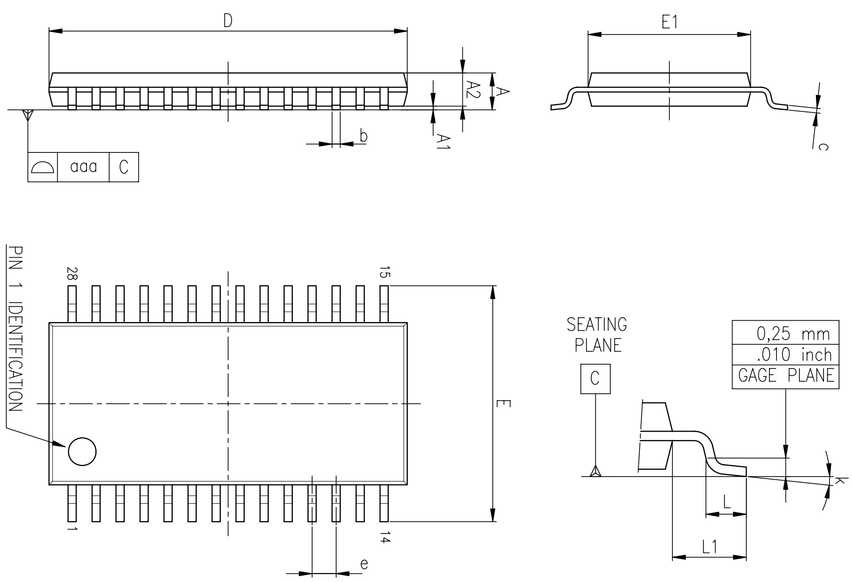
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.200			0.047
A1	0.050		0.150	0.002		0.006
A2	0.800	1.000	1.050	0.031	0.039	0.041
b	0.190		0.300	0.007		0.012
c	0.090		0.200	0.004		0.008
D [1]	9.600	9.700	9.800	0.378	0.382	0.386
E	6.200	6.400	6.600	0.244	0.252	0.260
E1 [1]	4.300	4.400	4.500	0.170	0.173	0.177
e		0.650			0.026	
L	0.450	0.600	0.750	0.018	0.024	0.030
L1		1.000			0.039	
k	0° (min.), 8° (max.)					
aaa			0.100			0.004

Note: 1. D and E1 does not include mold flash or protrusions. Mold flash or potrusions shall not exceed 0.15mm (.006inch) per side.

OUTLINE AND MECHANICAL DATA



TSSOP28
Thin Shrink Small Outline Package
JEDEC MO-153-AC



0128292 B

7 Revision history

Table 28. Document revision history

Date	Revision	Changes
16-Jul-2007	1	Initial release.
07-Jan-2007	2	Added and updated the values on the *Table 5: Electrical characteristics*. Document status promoted from preliminary data to datasheet.
30-Jul-2008	3	Updated *Table 5: Electrical characteristics*.
23-Apr-2009	4	Updated *Figure 1: Block circuit diagram on page 6*. Updated *Section 4.1: Input configuration on page 13*. Added *Section 4.1.2: Direct path on page 15*. Added *Figure 21: Switching characteristics on page 28*, *Table 9: I^2C bus electrical characterisitics on page 28* and *Figure 22: I^2C timing diagram on page 29*.